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Lee

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(54) **METHOD FOR FORMING A TRANSISTOR FOR REDUCING A CHANNEL LENGTH**

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(58) **Field of Classification Search** 438/163, 438/154, 180–181, 229–232, 585; 257/E21.433
See application file for complete search history.

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(57) **ABSTRACT**

A method of forming a transistor including: forming a gate oxide layer pattern and gate polysilicon layer pattern on a silicon substrate; forming a low energy ion implantation region aligned with both sidewalls of the gate polysilicon layer pattern; forming an amorphous region at a lower part of both sidewalls of the gate polysilicon layer pattern; reducing a channel length by removing the amorphous region so as to form a notch at a lower part of both sidewalls of the gate polysilicon layer pattern; forming a gate spacer at both sidewalls of the gate polysilicon layer pattern; and forming a high energy ion implantation region by high energy ion implantation of source/drain impurities into an entire surface of the silicon substrate including the gate polysilicon layer pattern and gate spacer.

6 Claims, 7 Drawing Sheets